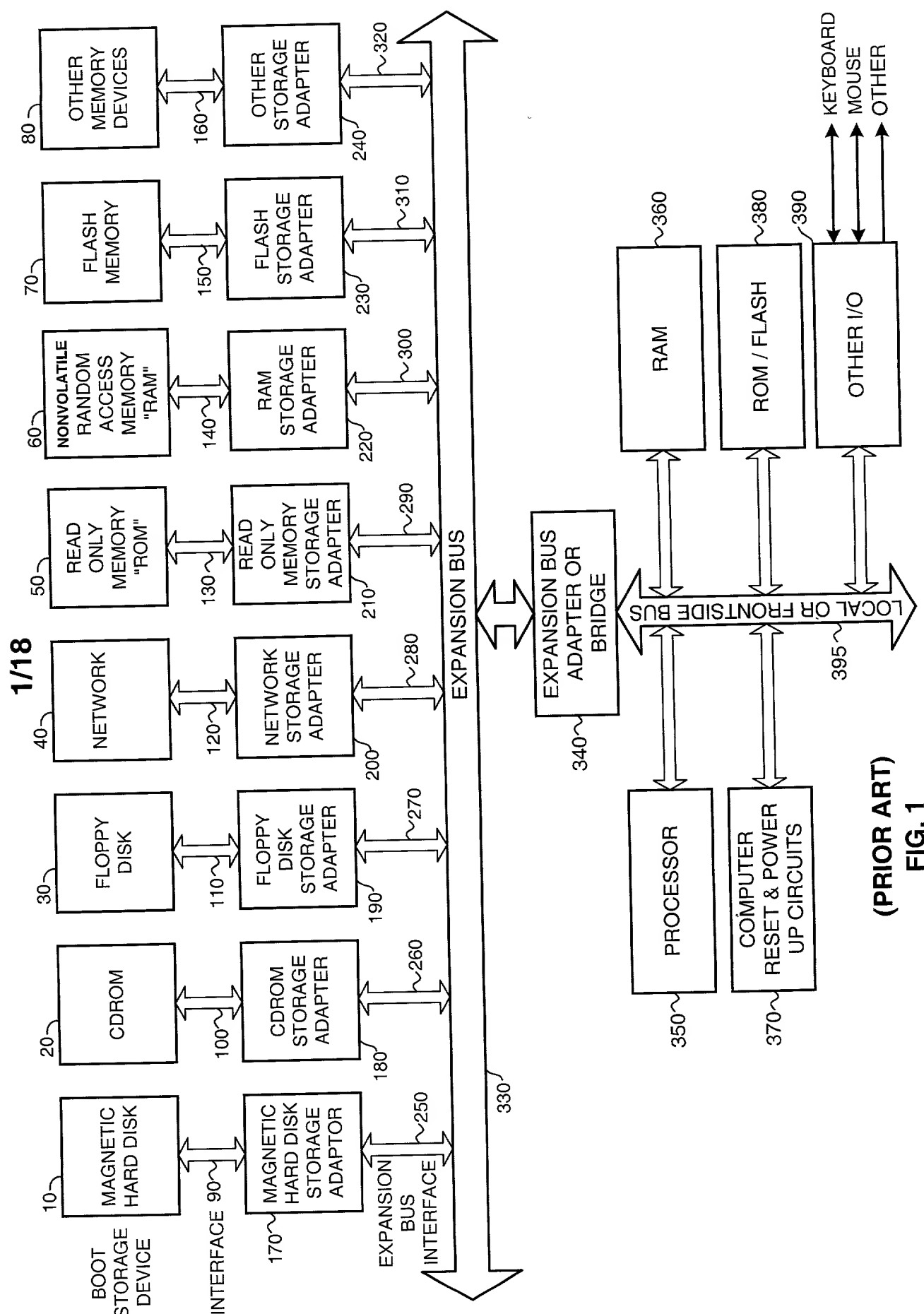
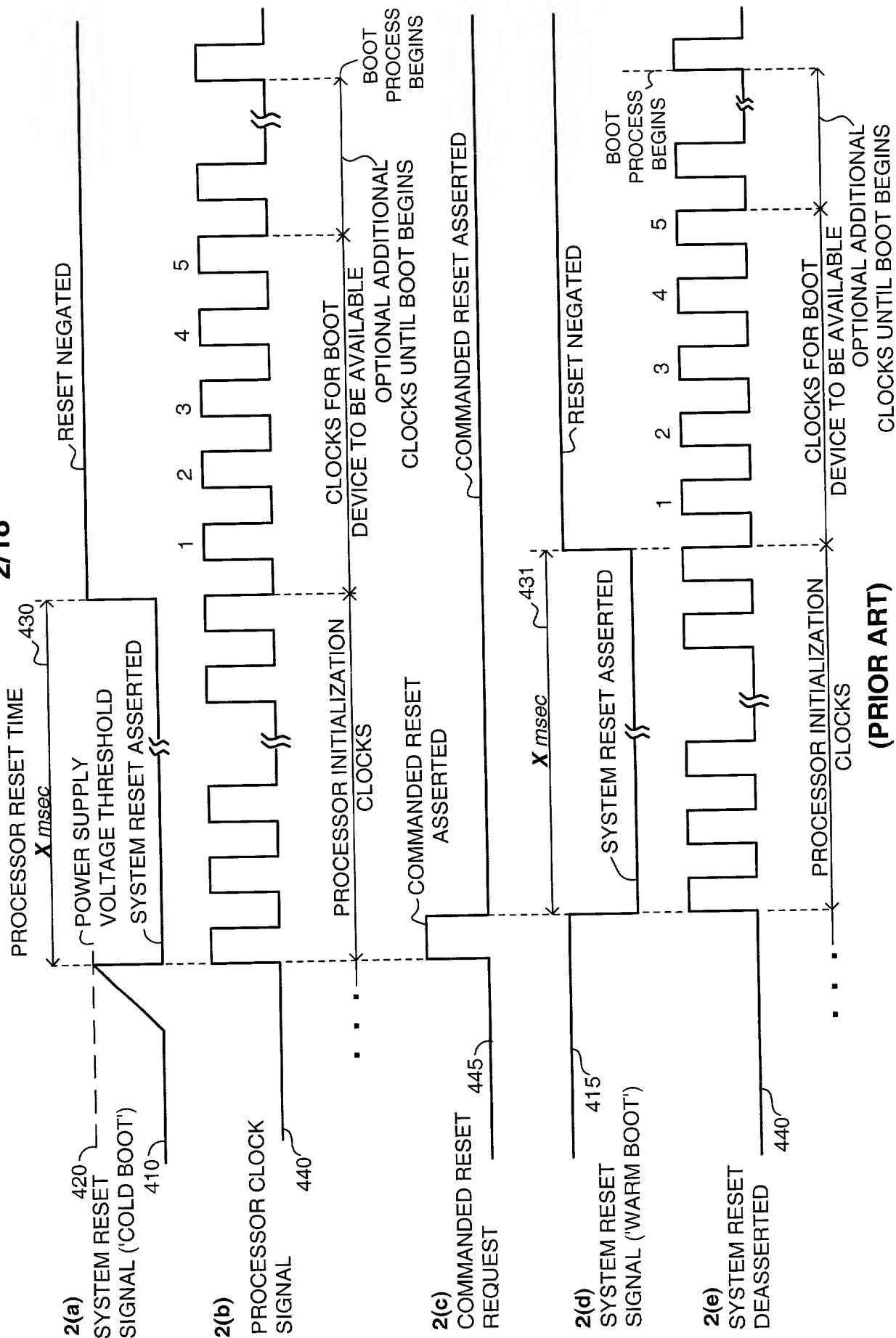


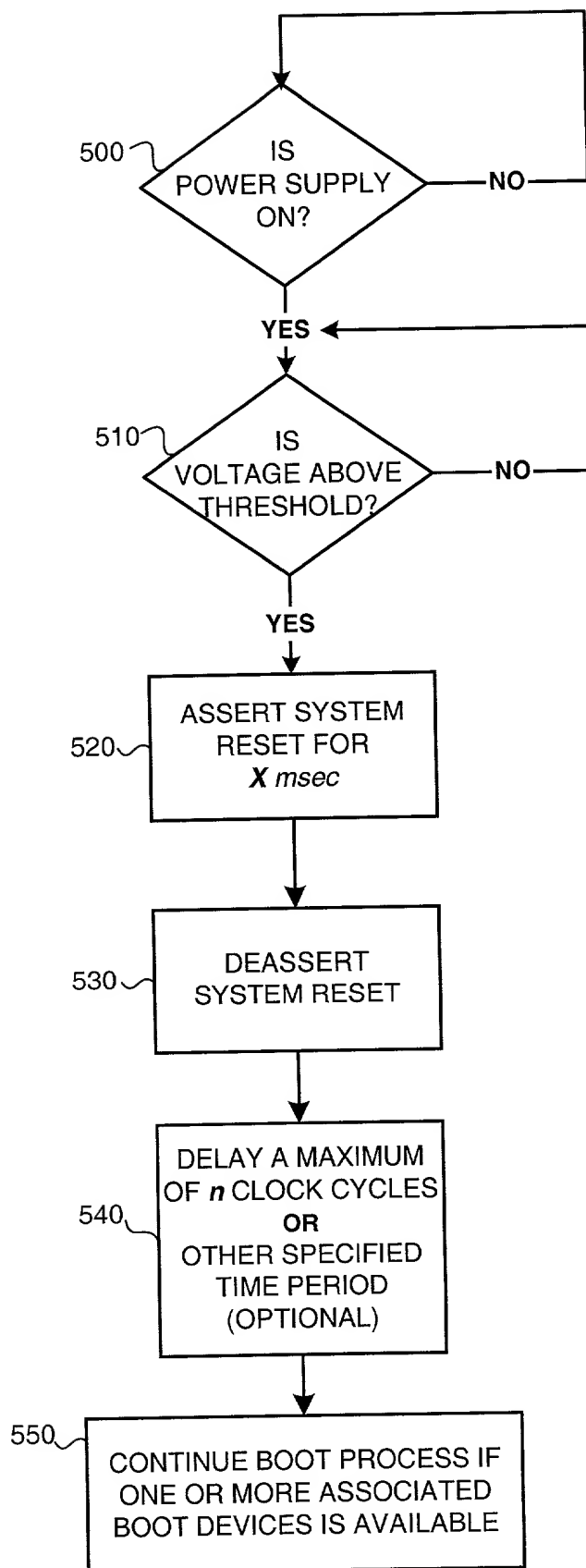
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(PRIOR ART)
FIG. 1

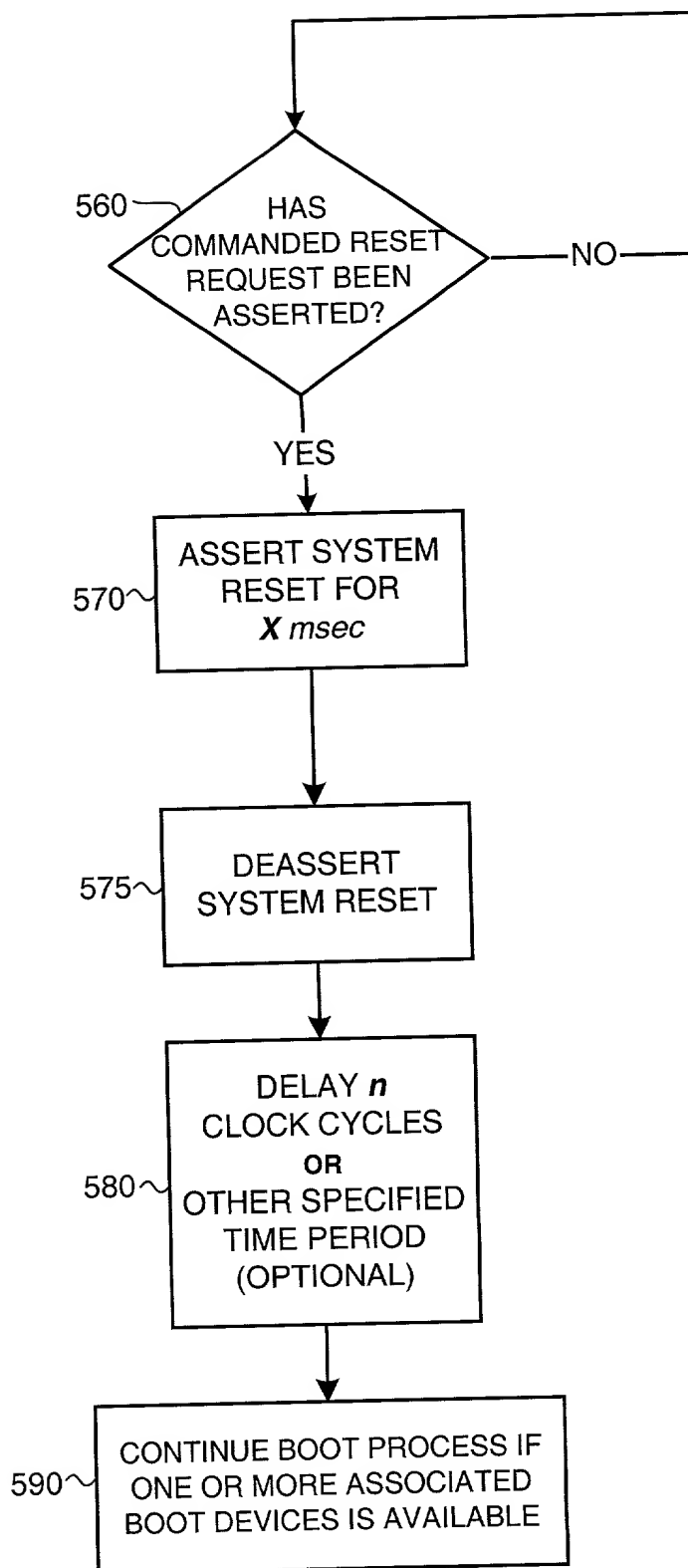


(PRIOR ART)
FIG. 2



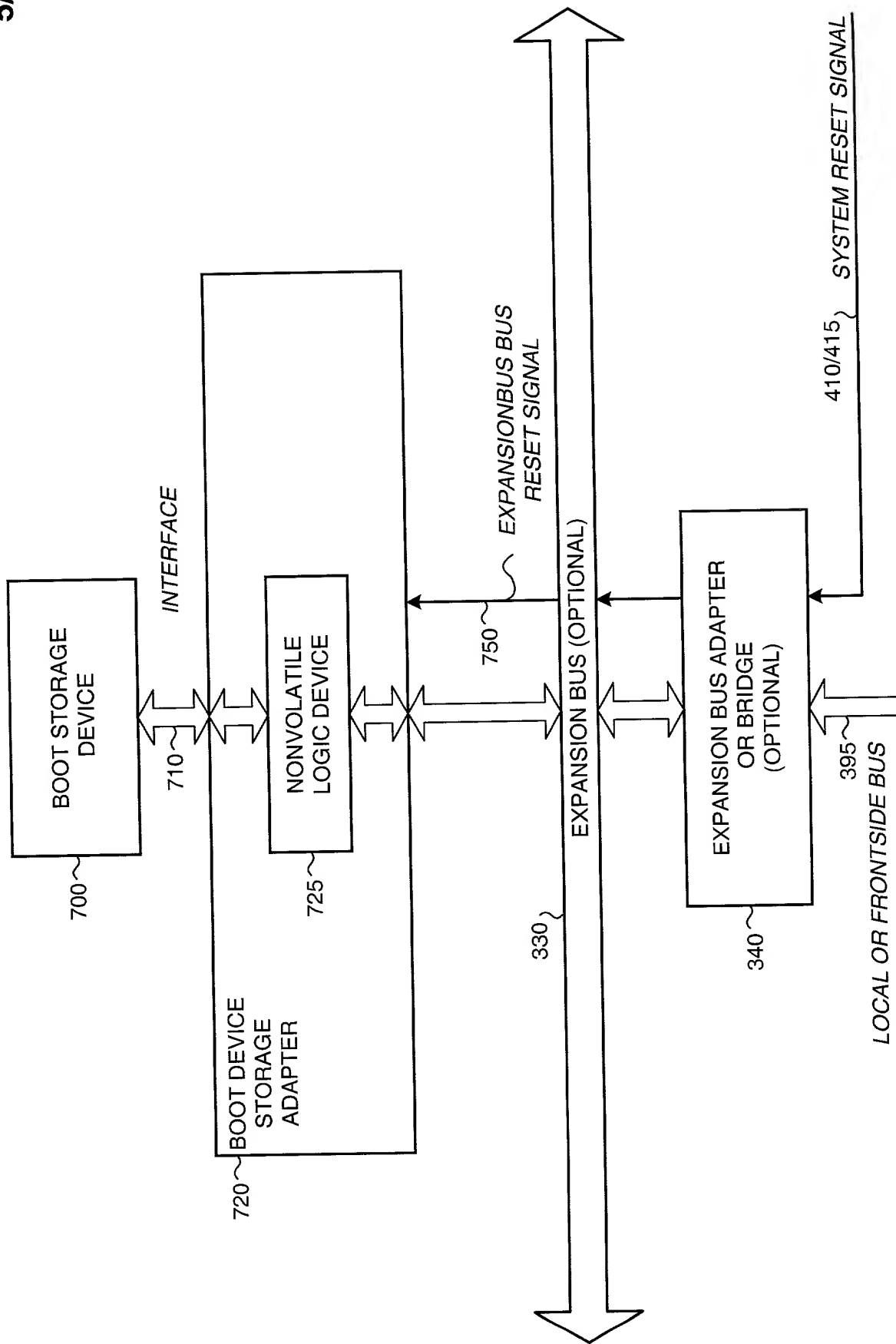
(PRIOR ART)

FIG. 3a



(PRIOR ART)

FIG. 3b



(PRIOR ART)
FIG. 4

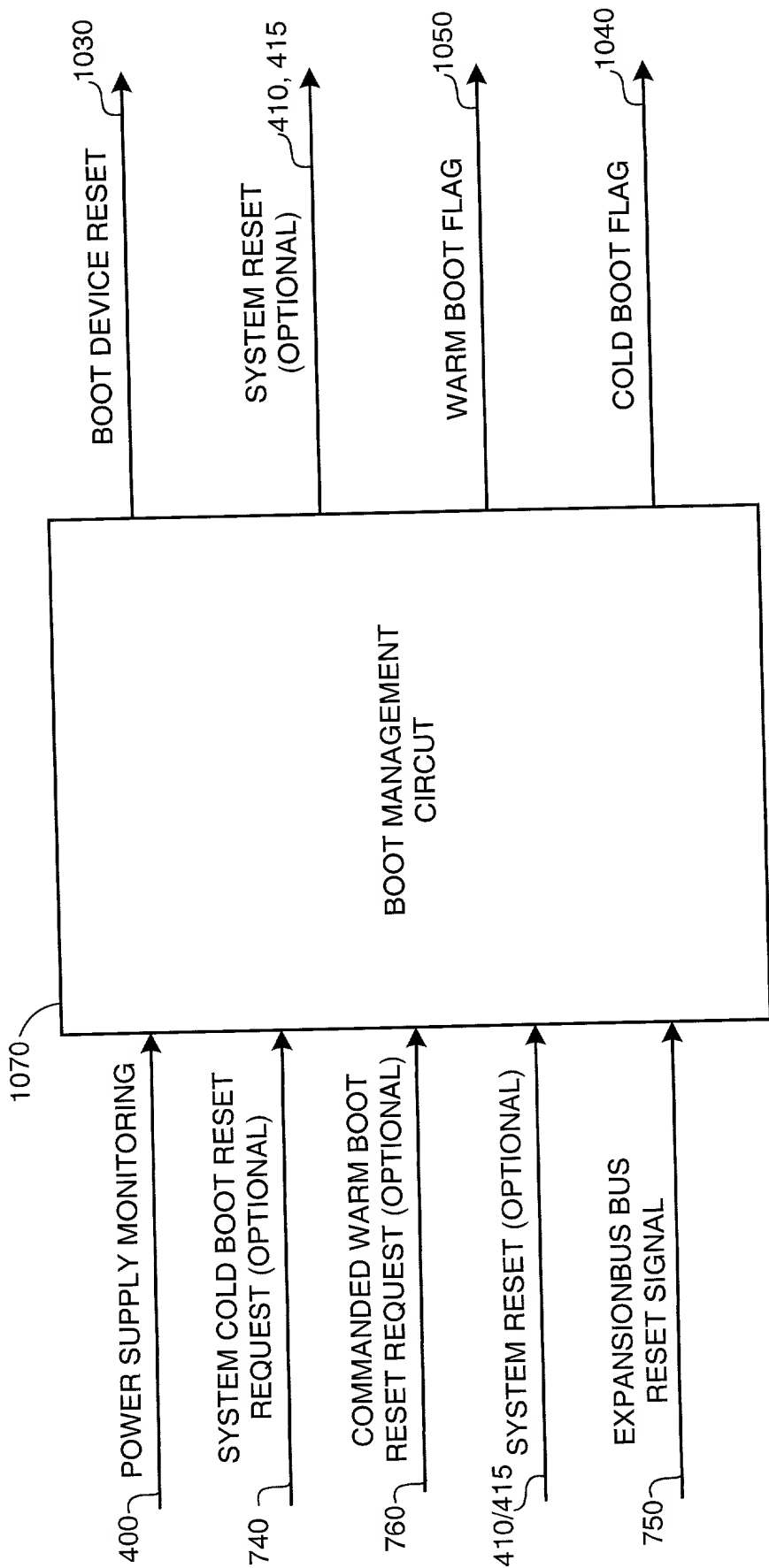


FIG. 5

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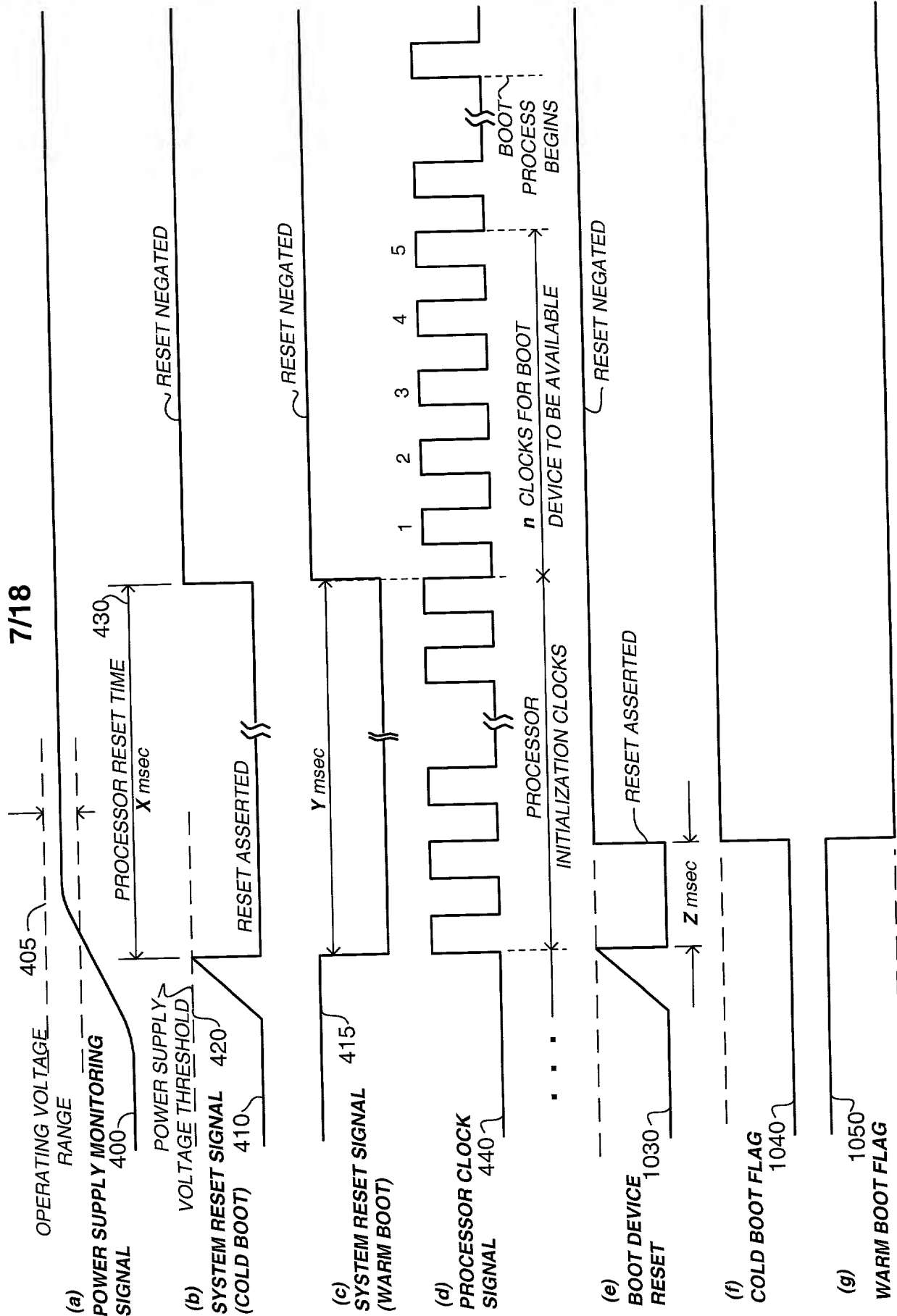


FIG. 6

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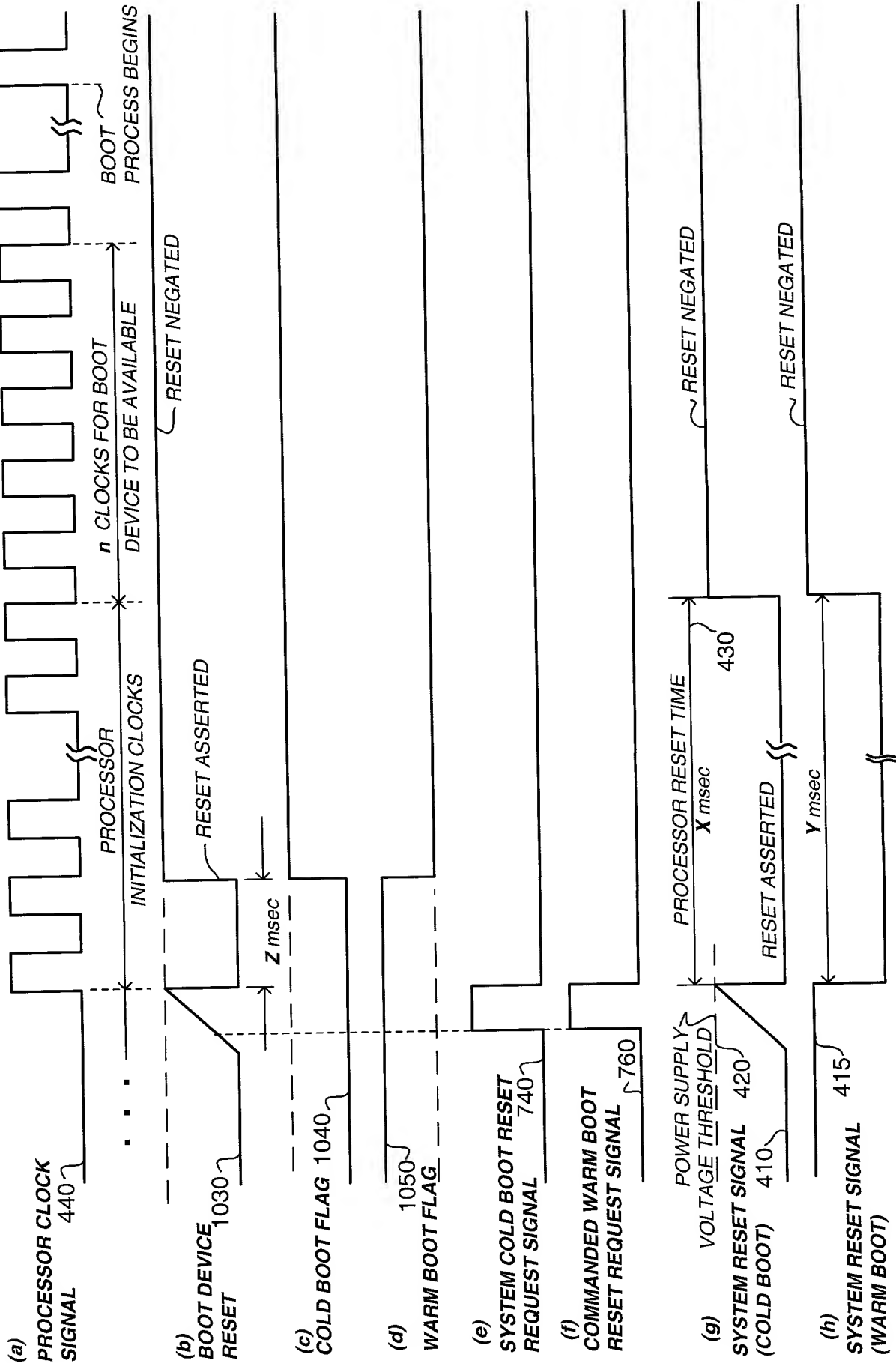


FIG. 7

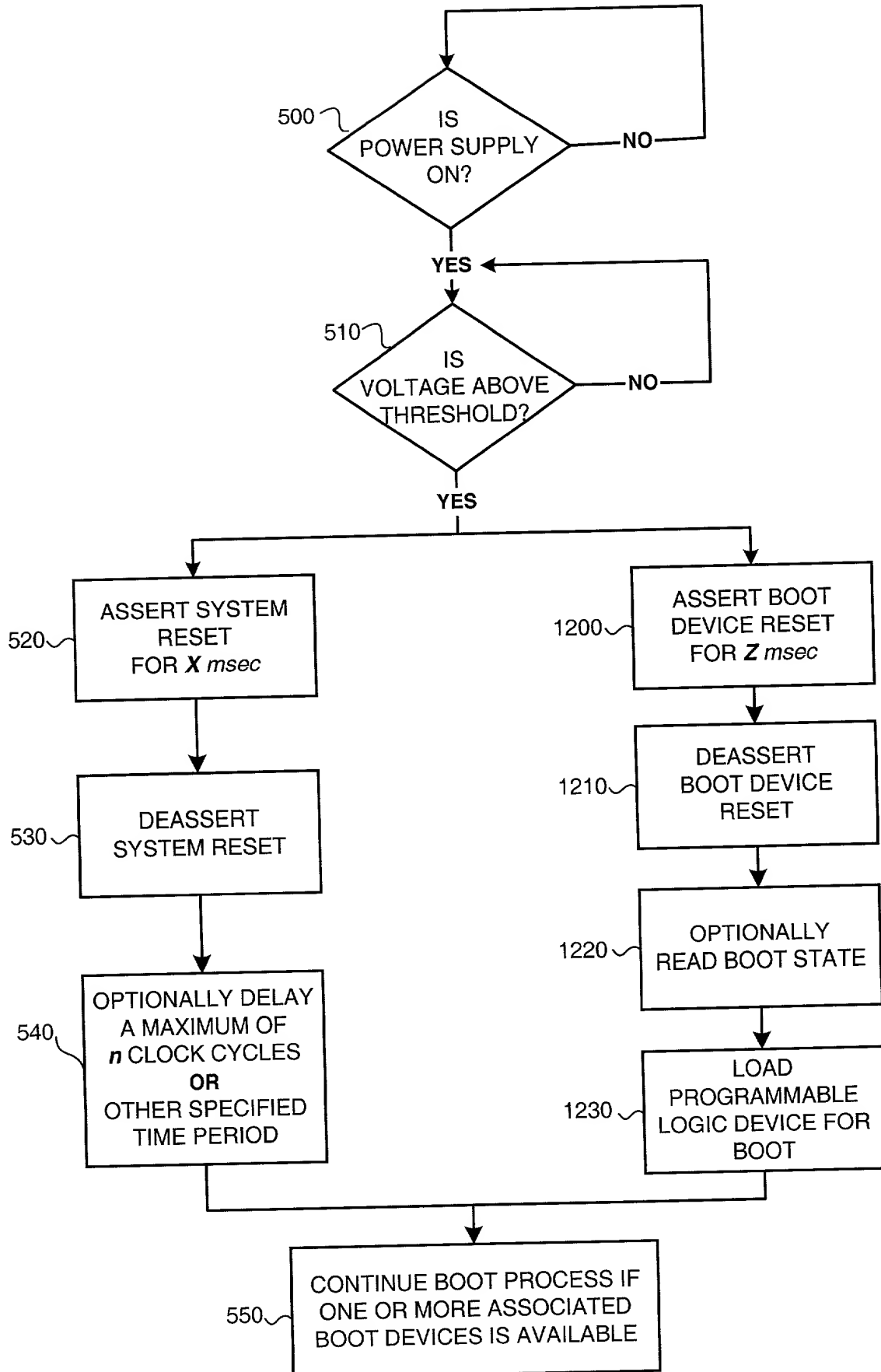


FIG. 8a

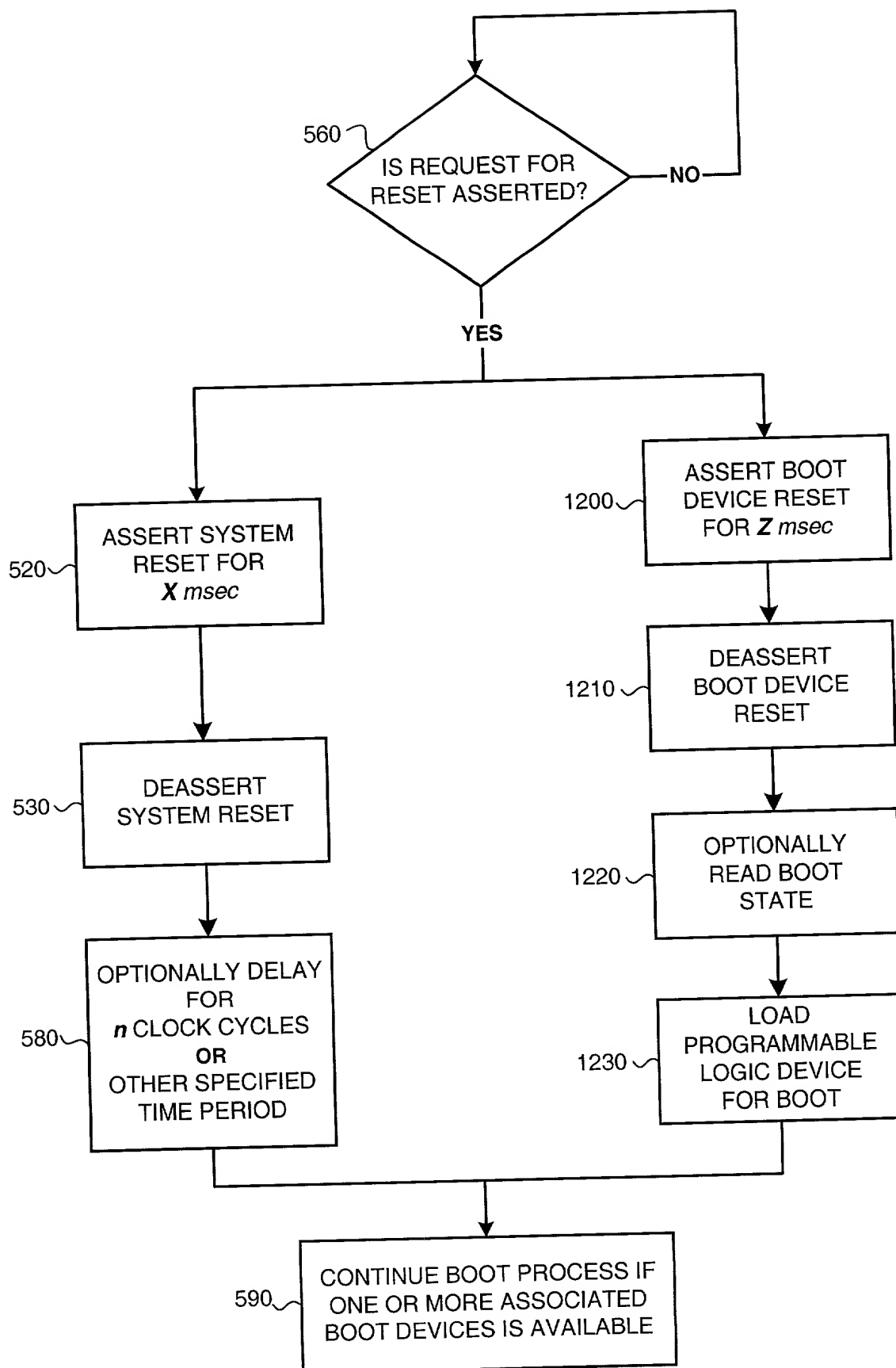


FIG. 8b

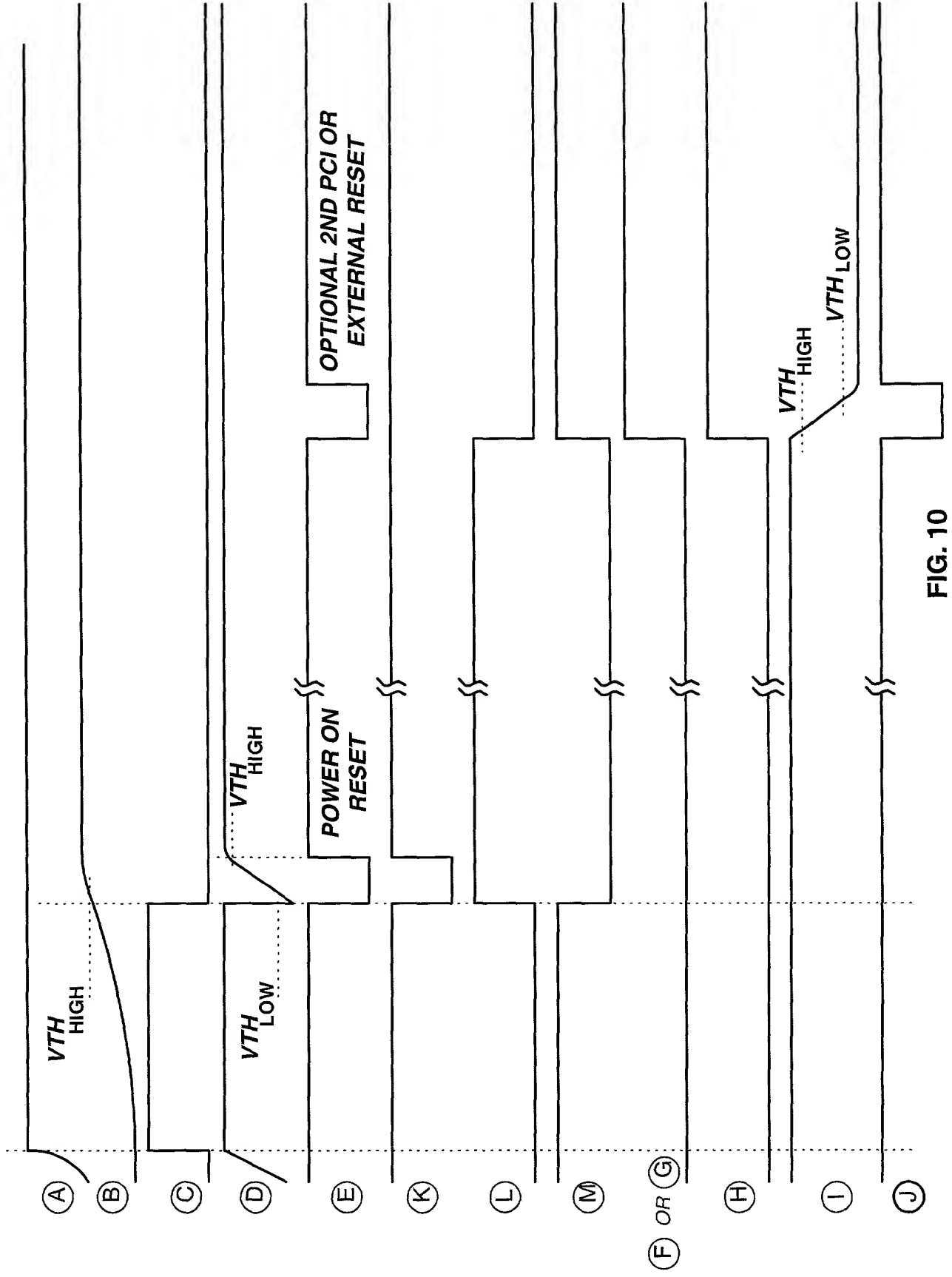


FIG. 10

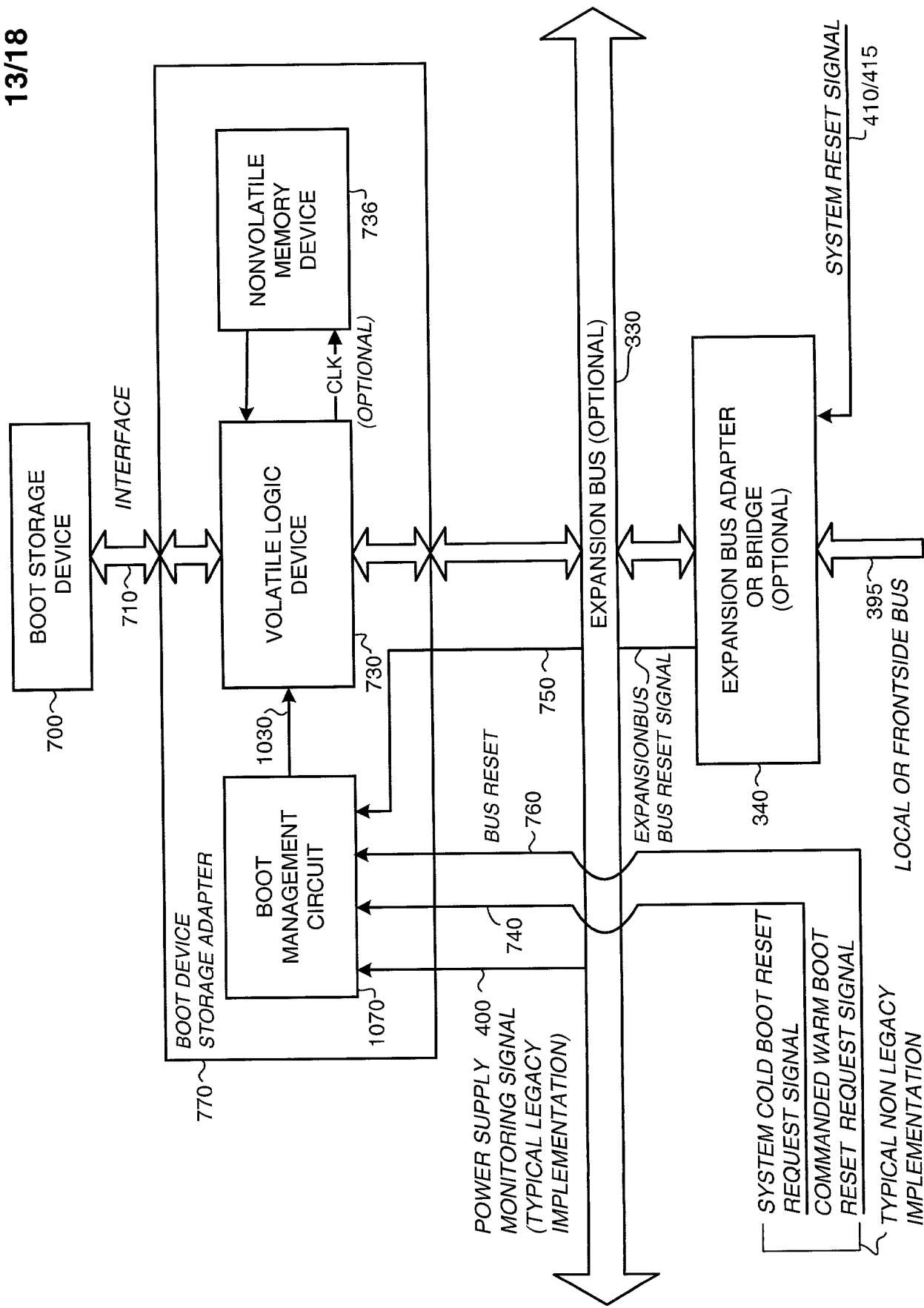


FIG. 11

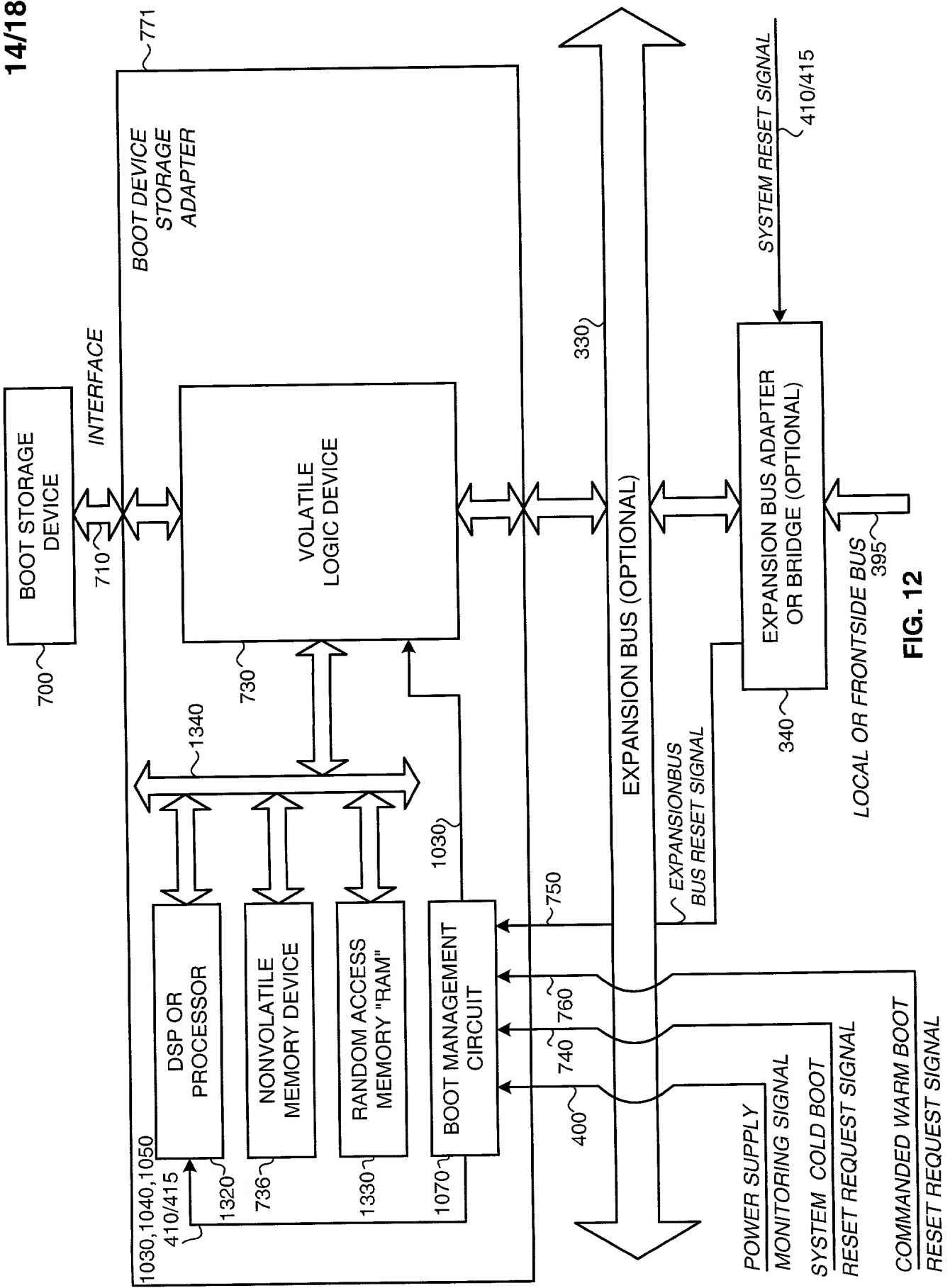


FIG. 12

FIG. 13 is a block diagram of a system architecture showing a boot management circuit (1070) connected to a boot storage device (700) and a volatile logic device (730). The boot storage device (700) is connected to an on-board non-volatile logic code (796) via an interface (710). The volatile logic device (730) is connected to a non-volatile memory device (795) via a boot device storage adapter (772). The system also includes an expansion bus (330) with an optional expansion bus adapter or bridge (340). The expansion bus (330) is connected to a local or frontside bus (395), which is connected to a non-volatile memory device (785). The boot management circuit (1070) is connected to the expansion bus (330) and the local or frontside bus (395). The expansion bus (330) also receives signals from a power supply monitoring signal (400), a system cold boot reset request signal (740), a commanded warm boot reset request signal (760), and an expansion bus reset signal (750). The expansion bus (330) outputs a system reset signal (410/415) to the non-volatile memory device (785).

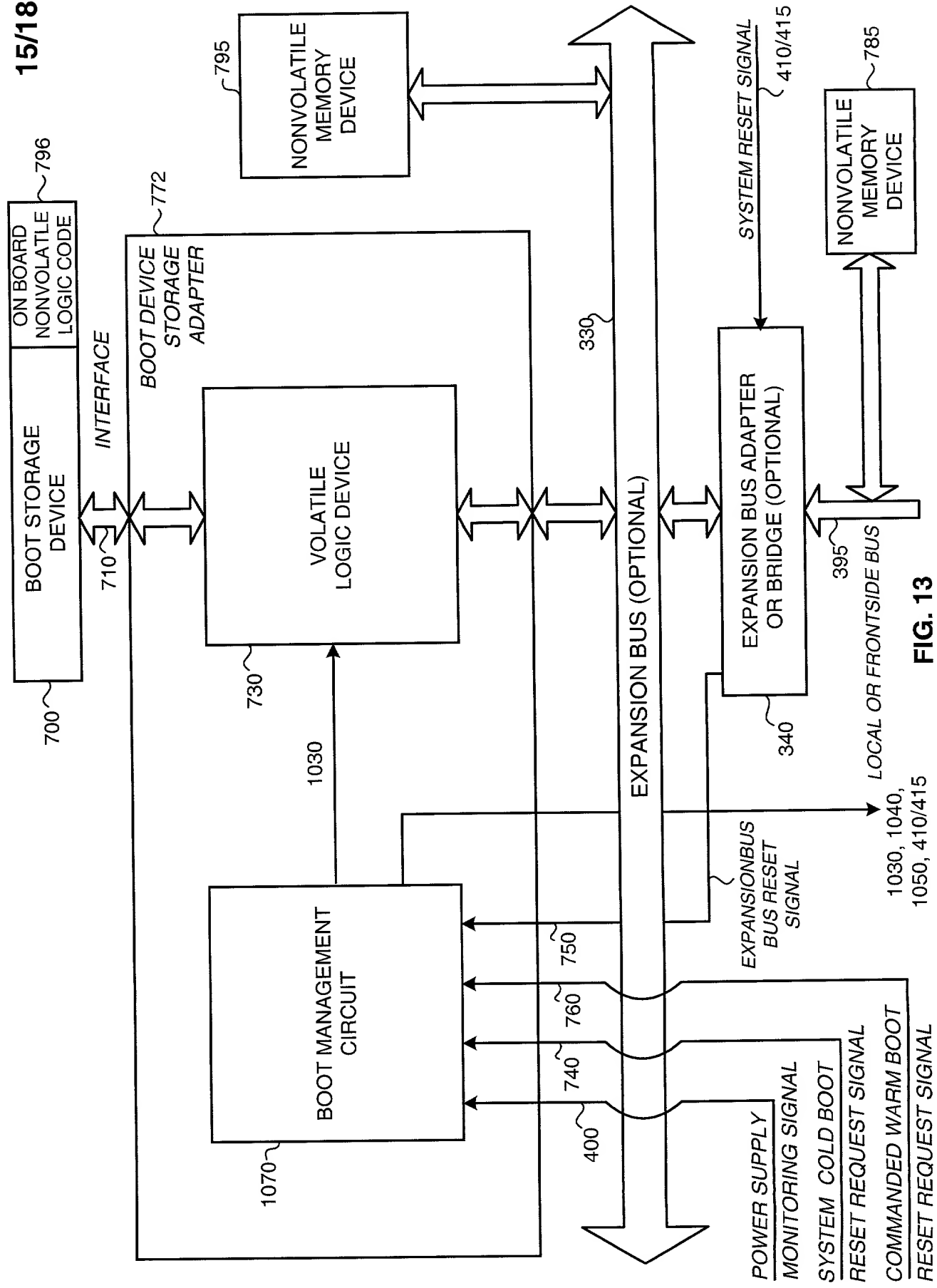


FIG. 13

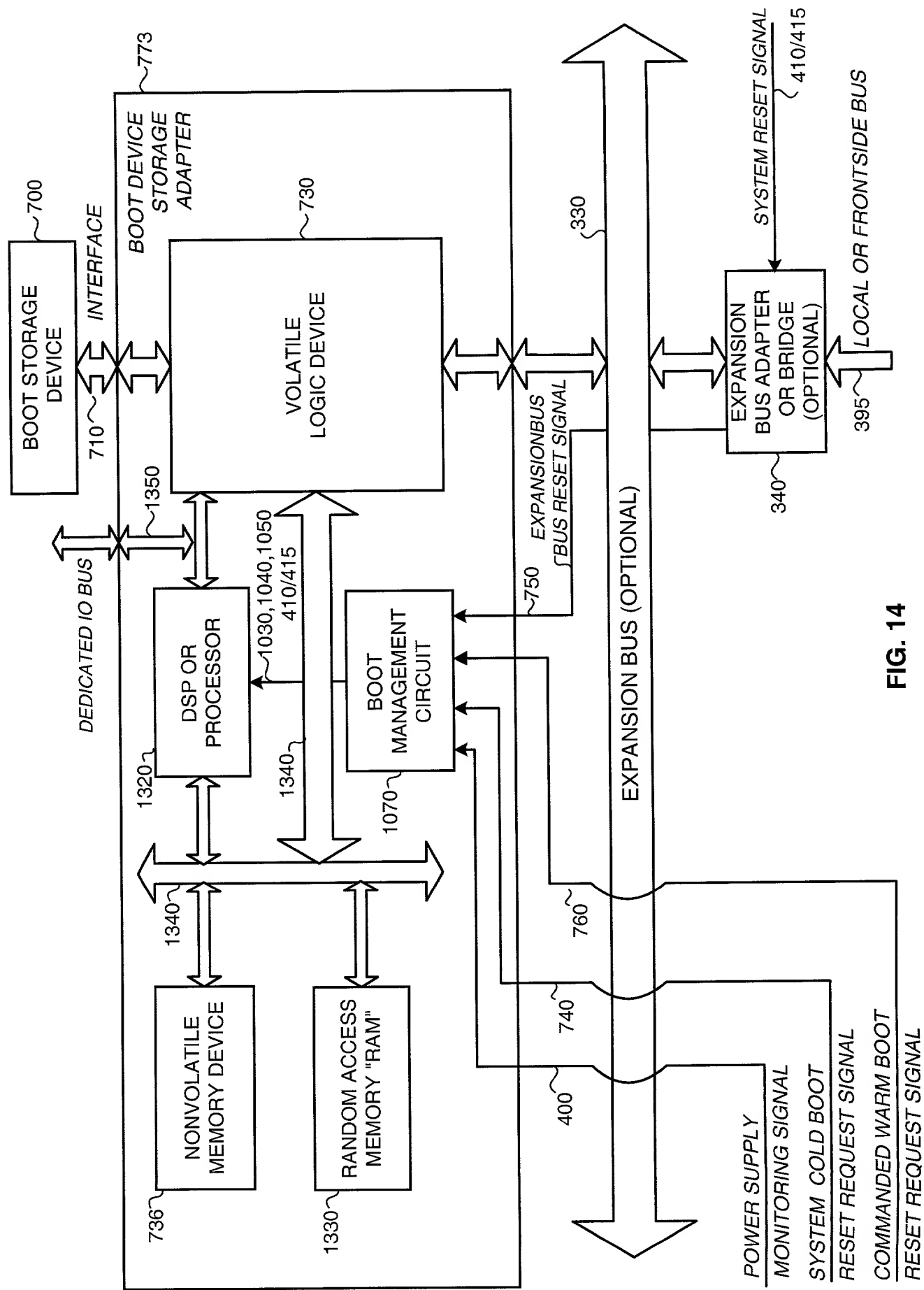


FIG. 14

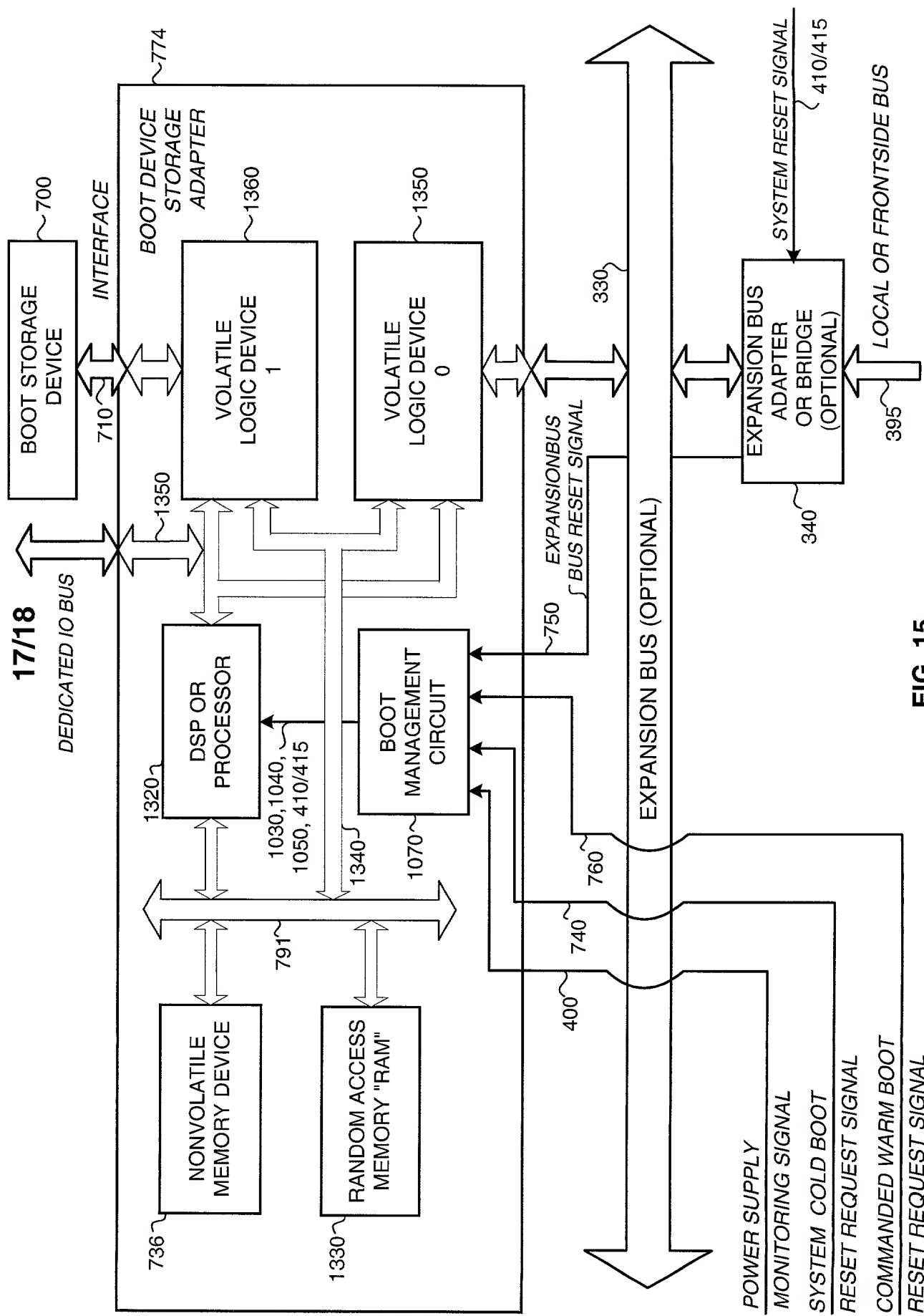


FIG. 15

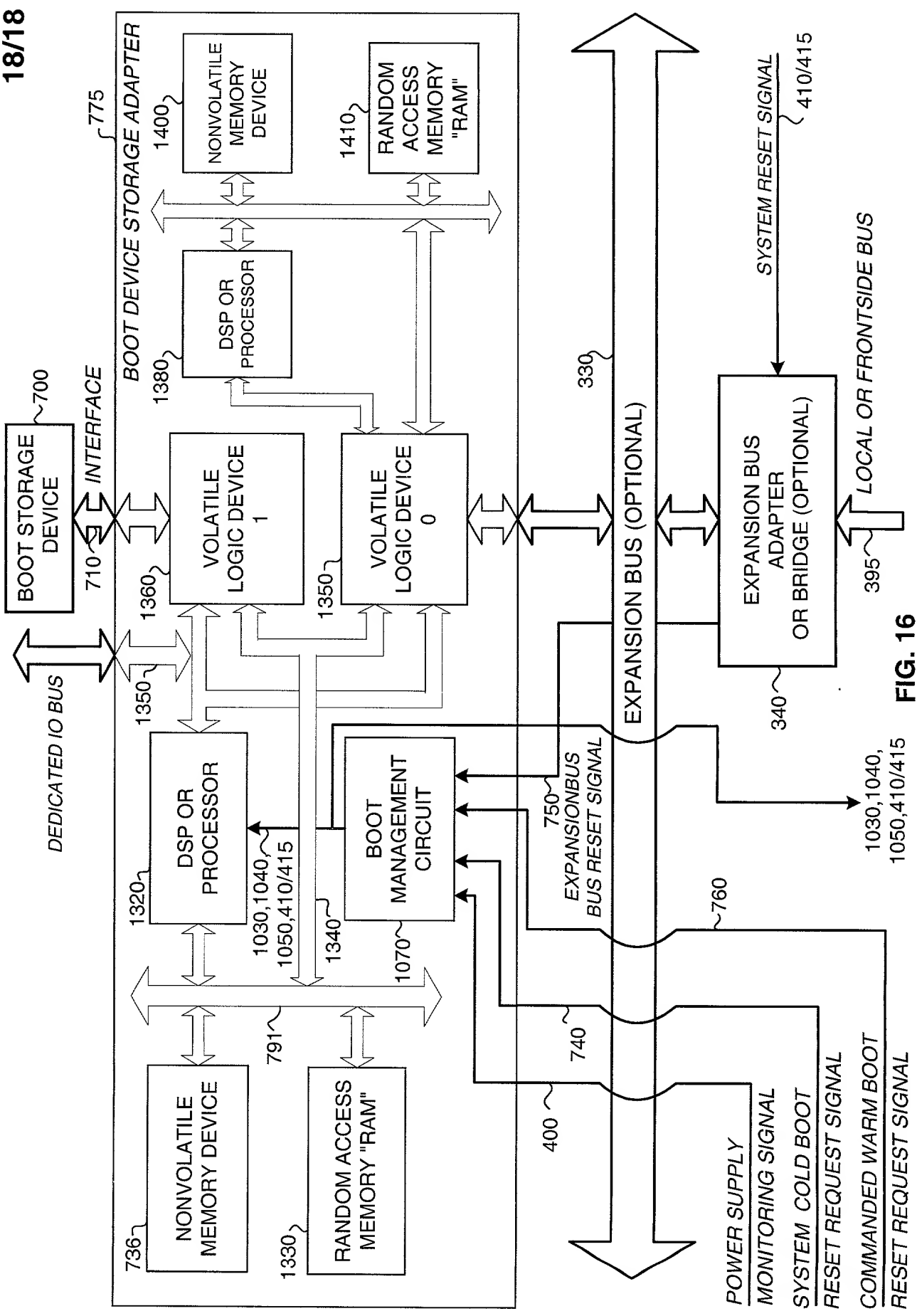


FIG. 16